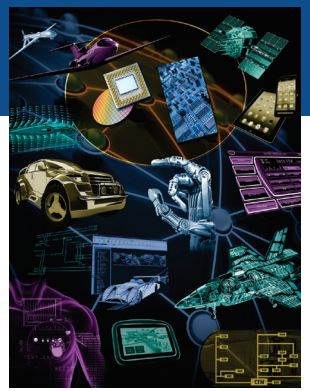
Mixed-signal Parasitic Extraction Flow using TSMC N16 and Mentor Calibre xACT Solution

Mentor, a Siemens Business / eTopus Technology

ABSTRACT

Silicon Valley startup company eTopus Technology, pioneer of ADC/DSP-based SerDes and leading designer of semiconductor products for enterprise network, data center and high-performance computing markets, are implementing their next generation of product offerings using TSMC 16nm technology. The success of their designs hinges on integration of sensitive analog/mixed-signal (AMS) elements within the context of complete designs. eTopus collaborated with Mentor, a Siemens Business, to adopt the Calibre® xACT™ parasitic extraction (PEX) solution, which they use extensively in their design flow. As a startup company, eTopus knows first silicon success is paramount, and the field solver accuracy around three-dimensional finFET devices provided by Calibre xACT PEX, combined with TSMC's advanced process technology, delivers a high level of confidence to design teams. This joint presentation between eTopus and Mentor describes some of the specific challenges presented by the design of a ring VCO, and how eTopus overcame these challenges, highlighting the flow from custom design tools through parasitic extraction into simulation.



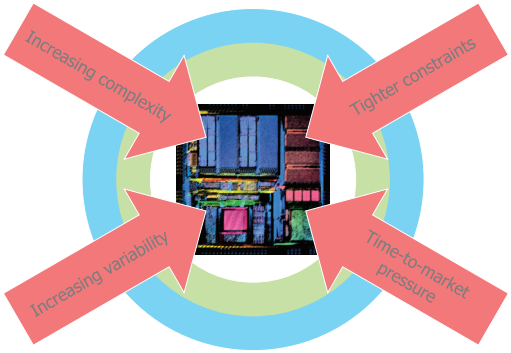
Mixed-signal parasitic extraction flow using TSMC N16 and Mentor Calibre xACT solution

Shahab Ardalan, eTopus Technology
Christopher Clee, Mentor

etopus Mentor A Siemens Business

Semiconductor Design Is Hard!

Job Stress Is Process Independent



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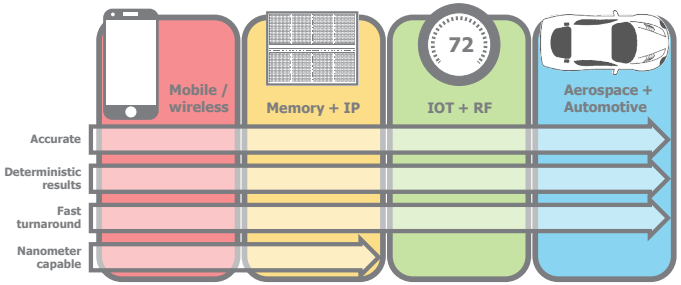
How To Define The Application Space For Extraction?



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It's Even Harder At 16nm And Below…

Multi-patterning
- Misalignment between masks leads to unpredictability
- Impact on parasitics is layout-dependent
- Effectively adds corners to analysis
- Creeping up to the routing layers

FinFETs
- No "one size fits all" solution
- 3D effects contribute significantly to parasitics, disrupt profile

Local interconnect
- Enables greater density, smaller standard cells
- Necessitates 3D device models

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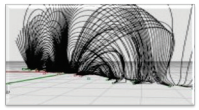
Rule-based Vs. Field Solver Approaches

Rule-Based / Table-based

- Measures distances between polygons, looks up values from pre-characterized tables
- Fast performance

$$C = \frac{\varepsilon A}{d}$$

Field Solver



- Solves Maxwell's equations
- Highest accuracy

$$\nabla \cdot E = 0 \qquad \nabla \times E = -\frac{\partial B}{\partial t}$$

$$\nabla \cdot B = 0 \qquad \nabla \times B = \mu\varepsilon \frac{\partial E}{\partial t}$$

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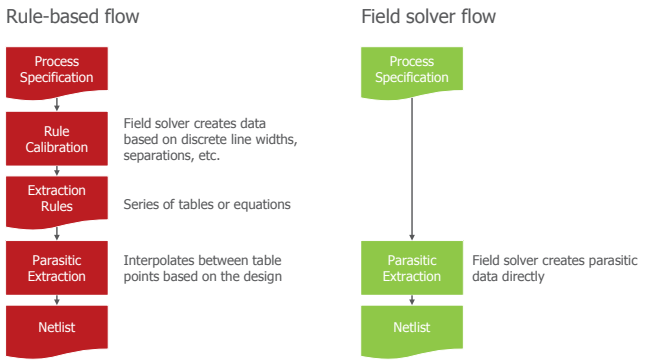
Parasitic Extraction Flows
(Simplified Overview)



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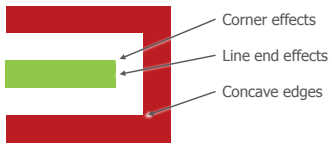
3D Line-End Effects

Long wires

$$C = \frac{\varepsilon A}{d}$$

Short wires



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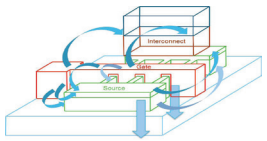
FinFET Challenges: Modeling MOL

More Parasitic Effects
- Further refinement by foundries

Complex Geometries
- Fin/poly/diffusion
- Local interconnect
- Contacts

Tighter Accuracy Requirements



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Parasitic Extraction >> Parasitic Calculation

- Parasitic effects
  - Intrinsic capacitance
  - Coupling capacitance
  - Resistance
  - Inductance
- Density
- Retargeting
- Manufacturing effects
  - Lithographic
  - CMP
- Reduction
- Device "ignore"s

$$C = \frac{\varepsilon A}{d}$$

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Impact Of Extraction Errors

- For analog design, tolerance control is particularly critical
- Transistor-level SPICE simulation gives performance within 3% of silicon when parasitic data is accurate
- 10-20% error in RC may lead to 5-15% error in delay
- Forces larger guard bands for timing and signal integrity

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Calibre xACT For Full-Chip Design
A New Approach

Table-based

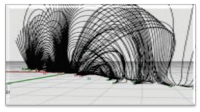
- Measures distances between polygons, looks up values from pre-characterized tables
- Fast performance

$$C = \frac{\varepsilon A}{d}$$

Hybrid Approach (Calibre xACT)

Best combination of performance and accuracy for advanced nanometer processes

Field Solver



- Solves Maxwell's equations
- Highest accuracy

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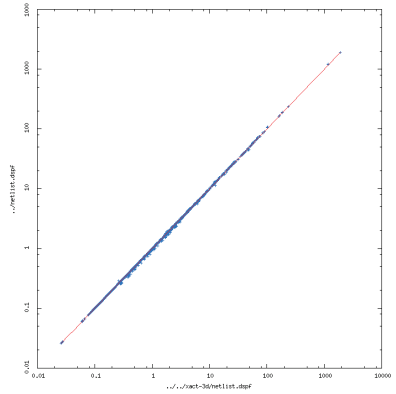
Calibre xACT Accuracy
N16 customer testcase



Calibre xACT vs. Calibre xACT 3D field solver	
Min	-13.1
Max	11.3
Mean	-0.1
Std dev	0.6

Filtered 5e-16

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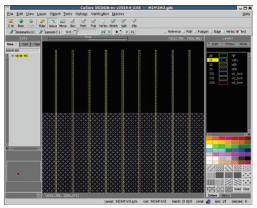
Calibre xACT Accuracy
Foundry test pattern vs. foundry golden

- All tools meet foundry qualification requirements
- Field solver has tighter standard deviation



Metric	Calibre xACT	Calibre xACT 3D field solver
Min	-5.5	-3.9
Max	3.2	2.1
Mean	0.1	-0.2
Std dev	1.5	1.1

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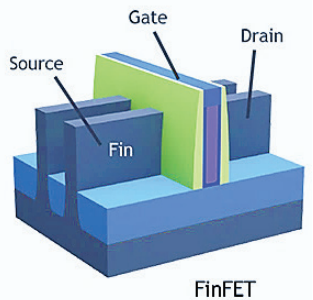
Why FinFet?

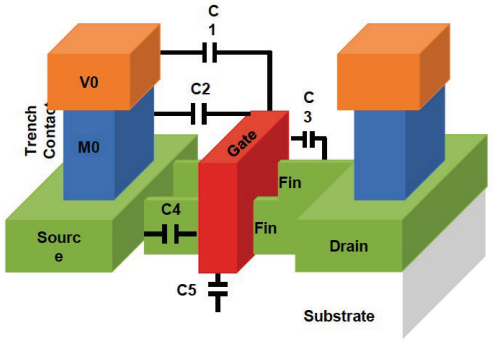
- g_{ds} , g_{bs} are much smaller
- g_m is higher
- Higher f_T
- Better NMOS and PMOS matching
- Perfect for digital circuits,
  - More monitoring, programmability & calibration
- More mismatch (smaller A_{VT})
- Higher parasitic
  - Resistance
    - Narrow wires
    - Looks like resistance becoming the dominant factor compare to par. cap.
  - Capacitance
  - Schematic simulation good for functionality test (par. estimation is a must)
- Hard to size
  - Quantized Width
  - Few choice on Length
- EM, Self-Heating and aging must be part of design flow



* Image: courtesy of Lam Research

Parasitic in FinFet

- Capacitance
- Resistance



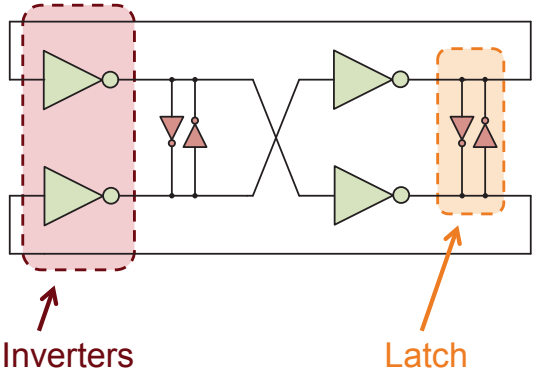
* Image: Daniel Payne

Case Study: Ring Oscillator

- A two stage ring oscillator has been selected as vehicular to examine the design flow.
- The test structure has been examined in different settings
  - Schematic Simulation
  - Schematic Simulation with pre-sim option
  - Post layout extracted simulation
  - Back annotated schematic
- Ring Oscillator free running center frequency has been selected as performance metric for comparison.

Ring Oscillator Architecture

- Two Stage Architecture
- Latch should be sized large to full fill the phase shift requirement for Barkhausen's criteria.
- Start-up is big issue as well as frequency therefore, accurate simulation is required.



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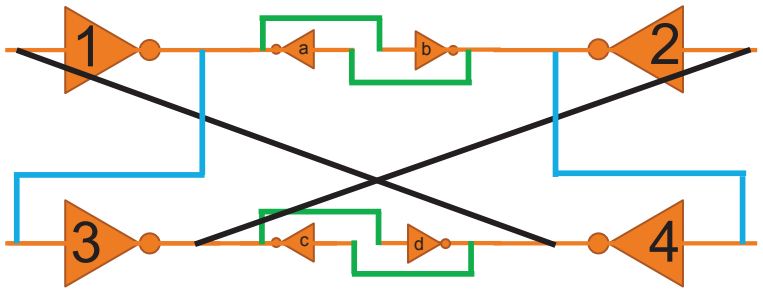
Floor Plan



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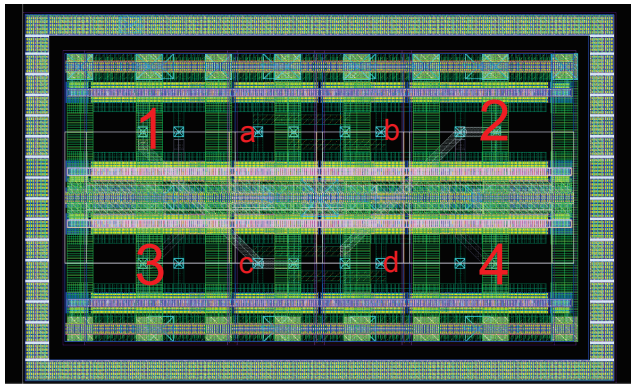
Layout



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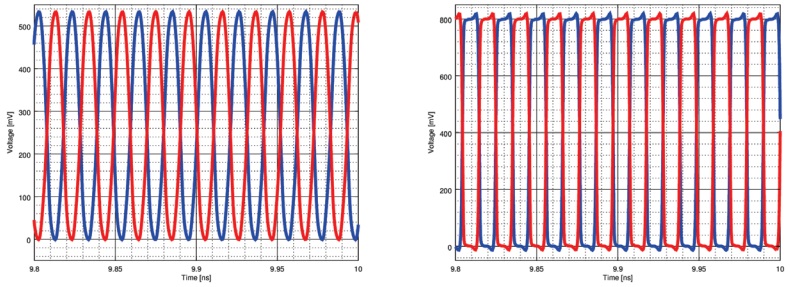
Simulation Results

- With disabled pre-sim
  - Frequency 48.5GHz



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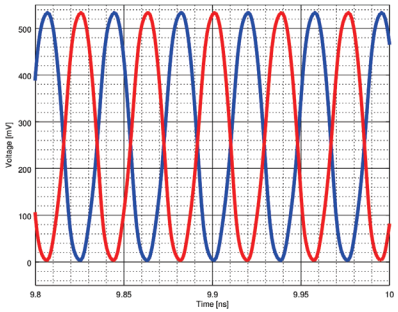
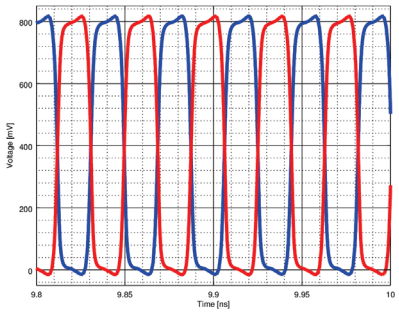
Effect of Pre-Sim

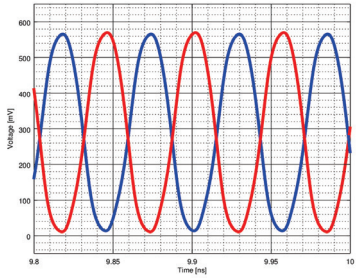
- With enabled pre-sim
  - Frequency 26.5GHz

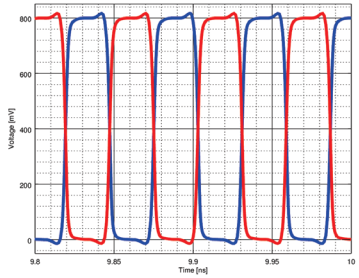




Extracted RC

- Extraction
  - RC Extracted
  - Majority of the delay is due to high resistance paths
  - Frequency 17.9GHz

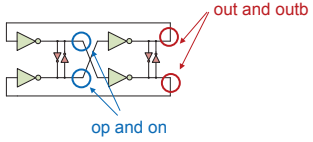


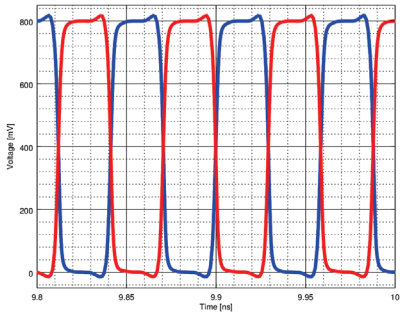


Back Annotated Schematic

Frequency 18.8GHz

Critical Node	Parasitic Cap
NET out	114fF
NET outb	115fF
NET op	111fF
NET on	110fF





Conclusion & Recommendation

Condition	Frequency
Schematic – No Pre Sim Option	48.5GHz
Schematic – With Pre Sim Option	26.5GHz
Extracted RC	17.9GHz
Cap Back Annotated Schematic	18.8GHz

- More than 100% error has been noticed between schematic simulation and extracted RC post layout simulation.
- Extracted simulation at the early stage of the simulation is mandatory to achieve optimum performance.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